CLAIMS

I claim:

1. A buffer for noise rejection in a logic circuit comprising:

an input node;

an output node;

a first inverter coupled to the input node, the first inverter having a first device size;

a second inverter coupled to the first inverter and the output node, the second inverter having a second device size at least six times greater than the first device size.

2. The buffer of claim 1 wherein the first and second inverters each comprise CMOS devices.

3. The buffer of claim 1 wherein the second device size is approximately ten times larger than the first device size.

4. The buffer of claim 1 wherein a ratio of the first device size to the second device size is in a range between 1:8 and 1:22.

5. A computer-aided method for design of a logic network comprising:

extracting parametric information from a layout of the logic network;

analyzing the logic network to identify a crosstalk-induced glitch at a node of a signal path in the logic network;

inserting a buffer at the node that functions to suppress a magnitude of the crosstalk-induced glitch, the buffer including first and second inverters coupled in

series, the first and second inverters respectively having a device size ratio of 1:6 or larger.

6. The computer-aided method according to claim 5 wherein the parametric information includes capacitance and resistance along the signal path of the logic network.

7. The computer-aided method according to claim 5 wherein the first and second inverters comprise CMOS devices.

8. The computer-aided method according to claim 5 wherein the device size ratio is in a range between 1:8 and 1:22.

9. The computer-aided method according to claim 5 wherein the device size ratio is approximately 1:10.

10. The computer-aided method according to claim 5 wherein the parametric information further includes timing slack available at the node of the signal path.

11. The computer-aided method according to claim 10 wherein the buffer has an associated delay that is smaller than the timing slack available at the node of the signal path.

12. The computer-aided method according to claim 5 wherein the node comprises an input of a logic state device.

13. The computer-aided method according to claim 12 wherein the logic state device comprises a flip-flop.

14. The computer-aided method according to claim 12 wherein the logic state device comprises a latch.

15. The computer-aided method according to claim 12 wherein the logic state device comprises a register.

16. A computer-aided method for design of a logic network comprising:

identifying a crosstalk-induced glitch at an input node of a logic state device in a signal path of the logic network, the crosstalk-induced glitch having a magnitude sufficient to disturb a logic level at the input node;

inserting a buffer in the signal path at the input node so as to suppress the magnitude of the crosstalk-induced glitch, the buffer including first and second inverters coupled in series, the first and second inverters respectively having a device size ratio of 1:6 or larger.

17. The computer-aided method according to claim 16 wherein the logic state device comprises a flip-flop.

18. The computer-aided method according to claim 16 wherein the logic state device comprises a latch.

19. The computer-aided method according to claim 16 wherein the logic state device comprises a register.

20. The computer-aided method according to claim 16 wherein the first and second inverters comprise CMOS devices.

21. The computer-aided method according to claim 5 wherein the device size ratio is in a range between 1:8 and 1:22.

22. The computer-aided method according to claim 5 wherein the device size ratio is approximately 1:10.

23. The computer-aided method according to claim 5 further comprising:

determining a timing slack figure at the input node, the buffer having an associated timing delay that is smaller than the timing slack.

24. A computer-readable storage medium having a configuration that represents data and instructions that cause a processor to:

extract parametric information from a layout of a logic network;

analyze the logic network to identify an input node of a logic state device in a signal path of the logic network where a crosstalk-induced glitch occurs;

modify the layout by insertion of a buffer in the signal path at or just prior to the input node, the buffer including first and second inverters coupled in series, the first and second inverters respectively having a device size ratio of 1:6 or larger.

25. The computer-readable storage medium according to claim 24 wherein the logic state device comprises a flip-flop.

26. The computer-readable storage medium according to claim 24 wherein the logic state device comprises a latch.

27. The computer-readable storage medium according to claim 24 wherein the logic state device comprises a register.

28. The computer-readable storage medium according to claim 24 wherein the device size ratio is in a range between 1:8 and 1:22.

29. The computer-readable storage medium according to claim 24 wherein the device size ratio is approximately 1:10.